AMENDMENTS TO THE CLAIMS

1. (Currently amended) A semiconductor test apparatus that tests the operation of a semiconductor based on a plurality of pattern data, comprising:

~~a memory for storing a plurality of pattern files each containing data;~~

a control unit for controlling the semiconductor test apparatus;

a disc apparatus and a buffer memory for storing a plurality of pattern files transferred from an external memory;

an executive memory comprising a pattern memory, an MIC memory, and an SPG (serial pattern generator) memory for executing tests for each type of semiconductor by applying test patterns and control data in the executive memories;

a ~~counter~~ counting device that counts the number of times ~~the~~ pattern data ~~of each of said pattern files~~ is used for each of said pattern files; and

~~a~~ said control unit ~~that produces~~ producing a pattern file use frequency count table showing the relationship between each of said pattern files and said number of times ~~said pattern~~ the files are used, and ~~stores~~ storing this pattern file use frequency count table in ~~said~~ a pattern file use frequency count table memory.

2. (Currently amended) A semiconductor test apparatus according to claim 1 wherein said ~~counter~~ counting device counts the number of times ~~each~~ said pattern ~~file of said plurality of pattern files~~ data is used in a set of tests for a predetermined number of semiconductors.

3. (Currently amended) A semiconductor test apparatus according to claim 1, wherein said control unit rearranges ~~said plurality of~~ the pattern files in descending order of frequency of use based on said pattern file use frequency count table after producing said pattern file use frequency count table.

4. (Currently amended) A semiconductor test apparatus according to claim 1, wherein said control unit deletes the pattern files in ascending order of frequency of use in the case

that the capacity of ~~an~~ said executive memory is insufficient when transferring said pattern files to the executive memory.

5. (Currently amended) A control method for a semiconductor test apparatus ~~that tests~~ comprising a disc apparatus, a buffer memory, and an executive memory comprising a pattern memory, an MIC memory, and an SPG memory, for testing the operation of a semiconductor based on a plurality of pattern ~~files each containing pattern~~ data, comprising the steps of:

counting the number of times said pattern data ~~of each said pattern file~~ is used for each pattern file; and,

preparing a pattern file use frequency count table that shows the relationship between each ~~pattern~~ file ~~of said plurality of pattern files~~ and each use frequency count corresponding to the number of times each ~~said pattern~~ file is used, and

storing ~~this~~ the pattern file use frequency count table in a memory.

6. (Currently amended) A control method for a semiconductor test apparatus according to claim 5, wherein, in said counting step, the number of times said pattern data ~~in each of said plurality of pattern files~~ is used in a set of tests for a predetermined number of semiconductors is counted.

7. (Currently amended) A control method for a semiconductor test apparatus according to claim 5, wherein said storing step stores ~~said plurality of~~ the pattern files in descending order of frequency of use based on said pattern file use frequency count table after producing said pattern file use frequency count table ~~is prepared~~.

8. (Currently amended) A control method for a semiconductor test apparatus according to claim 5, wherein said storing step deletes the pattern files ~~from said plurality of pattern files~~ in ascending order of frequency of use in the case ~~that the capacity~~ where capacities of ~~said~~

~~memory is~~ executive memories are insufficient when transferring said ~~plurality of~~ pattern files to ~~said memory~~ the executive memories.

9. (New) A semiconductor test apparatus comprising:

a control unit for controlling a plurality of memories for executing tests for a plurality of types of semiconductors;

a disc apparatus for storing a plurality of test pattern files for testing a plurality of semiconductors when test patterns are transferred from an external memory;

a buffer memory for storing a plurality of test patterns to be tested when the control unit transfers test patterns from the disc apparatus to executing memories comprising a pattern memory, an MIC memory, and an SPG memory, wherein

said pattern memory stores test pattern data for the rest of a semiconductor;

said MIC memory stores control data that control operations of the semiconductor test apparatus;

said SPG (Serial Pattern Generator) memory for storing pattern data and for sending the pattern of a periodic clock to a terminal of a semiconductor; and

a pattern file use count memory for storing a pattern file use frequency count table that shows the relationship between each pattern file and a use frequency count corresponding to the number of times these files are used, and storing this pattern file use frequency count table in the pattern file use frequency count table memory.

10. (New) A control method for a semiconductor test apparatus that is executed by a control unit for carrying out test performance of a semiconductor based on a plurality of pattern data, comprising the steps of:

storing a plurality of pattern data files corresponding to the test items for each type of semiconductor in a disc apparatus and a buffer memory;

distributing to an executive memory comprising a pattern memory, an MIC memory, and an SPG memory, a pattern data file used in the test for a semiconductor and

control data that controls the test from the test patterns after initializing each executive memory;

carrying out tests of semiconductors in accordance with the pattern data file;

counting the number of times said pattern data is used for each pattern file as a use frequency count of a pattern data file;

preparing a pattern data use frequency table that shows the relationship between each pattern file and a use count corresponding to the number of times these files are used;

storing the pattern file use frequency count table in a pattern file use frequency count table memory; and

deleting a pattern data file from the pattern memory which is the smallest use frequency count in the pattern file use frequency count data table in the case where the capacity of the executive memory is insufficient when transferring said pattern data files to the executive memory.